A2065 FUNCTIONAL SPECIFICATION

DESCRIPTION

The A2065 Ethernet LAN Card controller implements the 802.3 type protocol which calls for a 10 Megabit/sec CSMA/CD interface. It supports both 10Base2 Type B (Cheapernet) and 10 Base5 Type A (thick Ethernet) connections. The design has been developed around the AMD LANCE chipset which is comprised of the Am7990 Local Area Network Controller for Ethernet, the Am7992B Serial Interface Adapter, the Am7996 IEEE-802.3 Ethernet/Cheapernet Transceiver, and other associated logic necessary to implement a complete Ethernet interface.

ARCHITECTURE

A shared memory host interface was chosen because of the bus bandwidth requirements of the Am7990. A total of 32K of onboard buffering is provided to act as a shared interface between the Am7990 and Amiga CPU. This allows for worst case conditions of back to back Ethernet packets received by the board during loaded 68000 or graphics chip activity. In addition to the 32K of memory mapped packet memory, the Am7990's I/O registers are also mapped into the Amiga memory space as two sixteen bit locations. Finally, a small 256*4 Bit Prom is used to store the autoconfig data as well as the board's Ethernet address. The output side consists of both thick and thin (Cheapernet) Ethernet interfaces. The thick interface comes directly from the Am7992B SIA with transformer isolation. To implement the Cheapernet section, various passive components along with an Am7996 are required.

Functionally, the Ethernet interface may be partitioned into the following sections: Transceiver interface, autoconfig and configuration logic, Bus control buffers and logic, and onboard control logic/buffering including the packet memory. In the following sections each subsystem will be explored and discussed in more detail (refer to Figure 1).

TRANSCEIVER INTERFACE

The A2065 supports two types of cable media. The first type is commonly called "Thick Ethernet" or 10Base5. Thick Ethernet is used mainly in large installations where many nodes must be supported and distances between active repeaters are long. Typically, a transceiver box is physically connected to the Thick Ethernet backbone and a drop cable provides the actual connection to the LAN interface card present in the computer. The Thick Ethernet connection is actually a 15 pin Female D connector on the A2065 board. This physical interface is driven directly via transformer isolation by the Am7992B SIA. The transformers provide DC isolation and are designed to meet IEEE specifications. The function of the Am7992B is to decode/encode Manchester type serial data streams as per IEEE specifications for Ethernet. The key circuitry surrounding the Am7992B is the 20 MHz crystal (X1), which must meet exacting specifications, and the 5600 pF VCO Phaselock loop filter capacitor (C34). AMD data sheets call for a 5000 pF capacitor, but information from AMD applications engineers indicates that a value up to 6800 pF should be acceptable. Currently, this part is specified at 5600 pF ± 10% or better. Specifications for the 20 MHz crystal are set forth in the data sheet for the Am7992B. The jumper JP7 is supposed to affect the output signal for 802.3 applications. This jumper requires further testing and may need to be deleted for production. Thick Ethernet requires a +12V, 0.750A supply. This is supplied directly from the Amiga expansion connector. Note that a fuse is provided to protect against short circuits which might damage the Amiga or associated peripherals.

The second type of media is Cheapernet, commonly referred to as "Thin Ethernet" or 10Base2. Cheapernet evolved as a result of media costs associated with Thick Ethernet. Cheapernet allows for a "Bus" topology with up to 100 nodes. Inexpensive RG58 coax is used along with BNC T connectors and terminators. The Cheapernet section is comprised of the AM7996, a +5V to 9V DCDC converter, and various passive components which differentially drive the coax media and also act to recover the incoming data stream. The Cheapernet section also implements collision detection for collisions occurring on the media. Refer to the AM7996 data sheets for a complete technical discussion of the operation of the Cheapernet transceiver.

A2065 SYSTEM SCHEMATICS

AUTOCONFIG LOGIC AND CONFIGURATION LOGIC

Autoconfiguration is accomplished by reading the 256*4 AutoID Prom and relocating the physical base address of the Ethernet board within some 64K of Amiga I/O memory space. The autoconfig logic is implemented in the 16L8A PAL along with the Prom, the 74F521 address comparator, and the 74LS373 address latch. When the Ethernet board is ready for autoconfiguration, its _CONFIGIN line is brought low, address 0xE80000 is decoded, and a board select is generated. During the configuration process, the Prom parameters are read into memory to create the necessary system structure for the configed devices. It should be noted that the board serial number is used to generate the board's physical Ethernet address. The signal _IDP is generated from the 16L8A PAL to decode the Prom chip select. The read signal _RD to the Prom is generated from the 20L8A PAL. Refer to the PAL equations for details. Once the Prom has been read, the Amiga will write to address 0xE80048 to load the onboard address latch. The Ethernet board will generate a write pulse called SATL to load a 74LS373 with the board's new base address. The SATL signal comes from the 16L8A PAL. It is generated from a decode of 0xE80000 and a write strobe called _SWR. The _SWR strobe comes from the 20R6A PAL. It is essentially a delayed write pulse using delayed AS and the 7M Amiga clock. Once the latch is written, _CONFIGOUT is generated, enabling the output buffer of the 74LS373 latch. The board is now relocated and will respond to its new address.

BUS CONTROL BUFFERS AND CONTROL LOGIC

The Ethernet board data path consists of a 16 bit (D15:D0) wide data bus and is used for reading and writing the Ethernet local memory and the Am7990 registers. Only 4 bits (D15:D12) are significant with respect to the AutoID Prom. Referring to Figure 1, a pair of 74LS245 and 74LS244 isolate the Amiga's system bus from the internal Data/Address paths. Only the Amiga 68000 or the Am7990 can have access to this internal data/address path at one time. Normally, the Am7990 is burst DMA reading or writing the 32K memory as packets are being received or transmitted. The host 68000 requests access to this internal bus to either read/write memory or Am7990 registers. The 68000 accesses are arbitrated based on the Am7990 requiring the bus. A wait state is inserted to guaranty meeting 60ns _AS to XRDY delay during arbitration time. The bus control function is implemented by the 20R6A PAL. This PAL generates the data bus transceiver control _DBE. This signal is active when there is no exceptional conditions and a signal _ABE is active. _ABE is active only when the Am7990 is not requesting the internal bus (_HOLD, _LANCE not asserted). This satisfies the condition that a mutually exclusive relationship exists between the 68000 and the Am7990. The Ethernet board also listens on _BERR for bus faults; if _BERR is ever active, _DBE will not be active. The signal _LANCE is generated to enable the LS244 buffers which pass the Am7990 DMA address thru to the Ram buffers. _LANCE in conjunction with _ABE determines which source (68000 or Am7990) drives the internal address path. The Am7990 works in a multiplexed address/data method. First an address is latched during the first part of the read/write cycle, then the actual data transfer occurs.

ONBOARD CONTROL LOGIC/BUFFERING

The onboard control logic consists mainly of chip selects and read and write strobes to memory and the Am7990. The 32K buffer is partitioned into a high bank and a low bank of 8K * 16 bits each. Address line A14 determines which bank is active. The read and write strobes to the memory are qualified by bus control signals. During 68000 R/W cycles, the signals READ, _UDS, and _LDS are used from the system bus along with _BSEL to control reading data. These same signals plus one generated onboard called _ENDCYC are used to generate write pulses. _ENDCYC is generated by the 20R6A PAL. During Am7990 bus ownership, a different set of signals controls the R/W timing pulses. All these control signals are generated within the 20L8A Internal Bus Control PAL. The 20L8A PAL also generates chip selects for the 32K memory and Am7990 I/O register. For further information, refer to the PAL equations and the Am7990 data sheet.

LOW LEVEL INTERFACE PROGRAMMING

For a complete discussion of programming the Ethernet board, refer to the Am7990 application sheets and the Ethernet device driver source. A brief explanation is given here. The Amiga configures the board and builds a config structure in memory. The Ethernet software goes out and finds the location of the board and reads the serial number. The serial number plus the manufacturer base Ethernet address make up the complete Ethernet address. The software then sets up the initialization block in the 32K memory which sets up two circular linked list buffers, one transmit and one receive queue. The initialization block refers to these queues as "descriptors". The Am7990 is then programmed via I/O transfers into internal registers for various network and operational parameters, along with the setting up of an interrupt handler. Finally, the action starts. The network layer software fills buffers to transmit, while emptying buffers that are filled from incoming packets.

A2065 ETHERNET BOARD MEMORY MAP

Amiga Address	Size	Usage
xx0000	256 bytes	Autoconfig Prom Contains standard autoconfig data and Ethernet address. Upper data byte only, i.e. D15-D12. Readable before and after autoconfig.
xx4000	4 bytes	LANCE Ethernet controller chip xx4000 Register address port (RAP) xx4002 Register data port (RDP)
xx8000	32K bytes	32K Packet Buffer

Notes: xx denotes upper address after autoconfiguration location (initially base board address appears at hex E80000).

The Autoconfig Prom is read only. It lies on data lines D15-D12. The serial number portion is used to hold the user specific portion of the Ethernet address. This partial address is concatenated with the vendor portion of the Ethernet address to form a full 6 byte address.

The Register Data Port and Register Address Port are defined in the Am7990 data sheets.

The 32K buffer is organized as 16K by 16 bits for word/byte, read/writes. This buffer is managed and initialized as per the Am7990 LANCE data sheets.

The board is decoded into two 16K chunks and one 32K chunk. Total size is 64K.

A2065 ETHERNET BOARD JUMPERS

When the shunt plug is inserted into a jumper position, the corresponding signal is active.

Interrupt Jumpers

JP1 INT1
JP2 INT2 (default setting)
JP3 INT4
JP4 INT5
JP5 INT6
JP6 INT7

Am7992 Transmit Mode Jumper

JP7 Transmit mode select. Default is to leave shunt plug out. See the Am7992 data sheets for actual usage.

Thick Ethernet/Cheapernet Jumper Block

ABC When the AB jumper is connected with the shunt block, Cheapernet is selected; otherwise, the connection of the BC jumper will select Thick Ethernet.

ENVIRONMENTAL TEST REQUIREMENTS

Units shall comply with the following environmental resistance requirements.

TEMPERATURE	
Operational	5 to 55°C
Storage	−20 to +70°C
Gradient	+10°C/hour
Temperature Cycle	−20 to 60° C, 10 cycles, 10 minutes minimum at each extreme, 5 minutes maximum between extremes
HUMIDITY	
Operational (relative)	10 to 90% (non-condensing)
Storage (relative)	5 to 95% (non-condensing)
VIBRATION	
Non-operating (randomfrequency)	5.2 Gs per MIL-STD 202 Method 214, 15 min. in each of three axes
SHOCK	
Operational	5 Gs to each of 6 axes, two 11 mSec half sinewave shocks
Non-Operational	20 Gs applied as above
ALTITUDE	
Operational	0 to 3,000 meters
Non-Operational	0 to 15,000 meters

A2065 SYSTEM SCHEMATICS

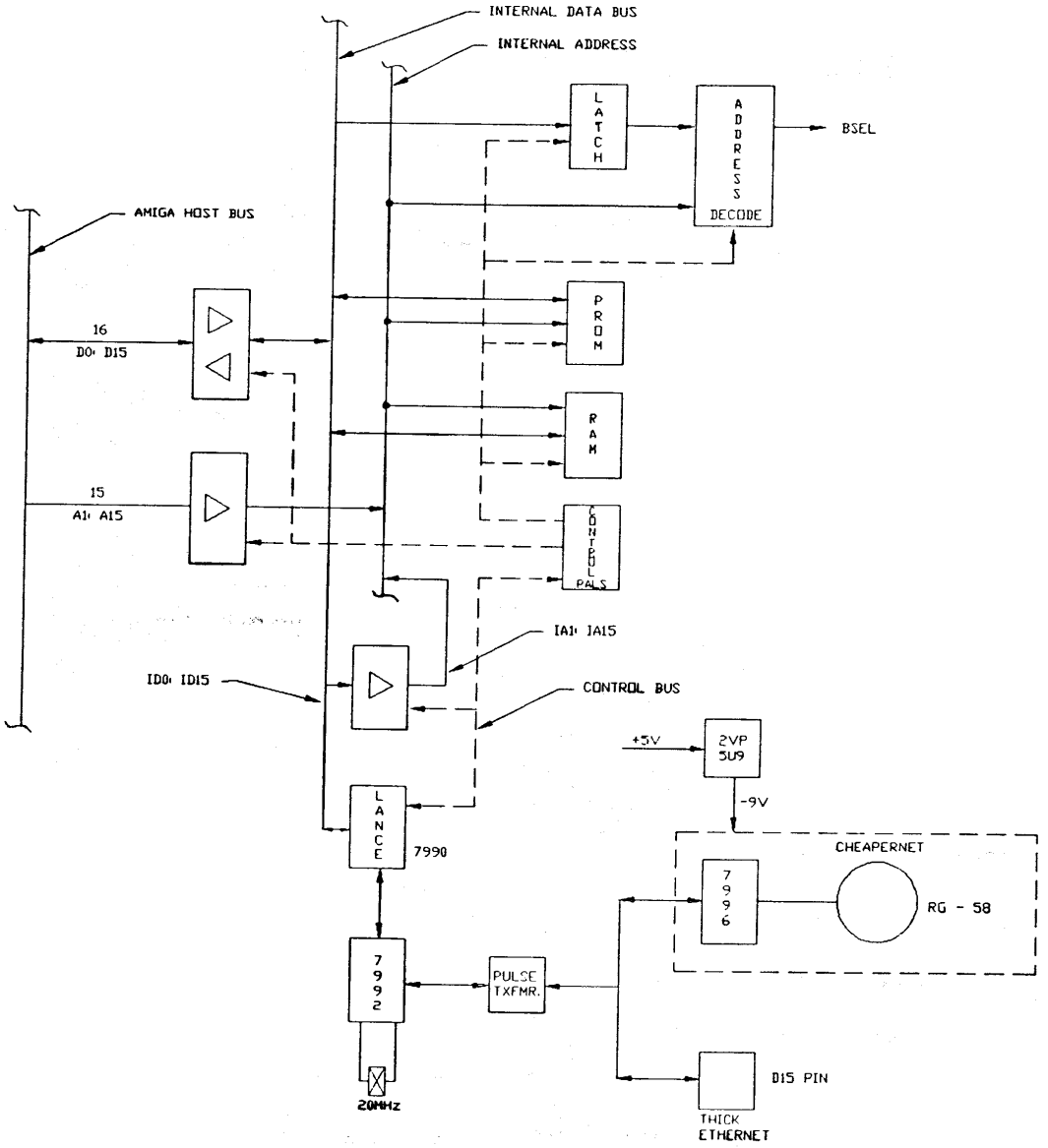


FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

Commodore International Spare Parts List
SHIPPING ASSEMBLIES

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

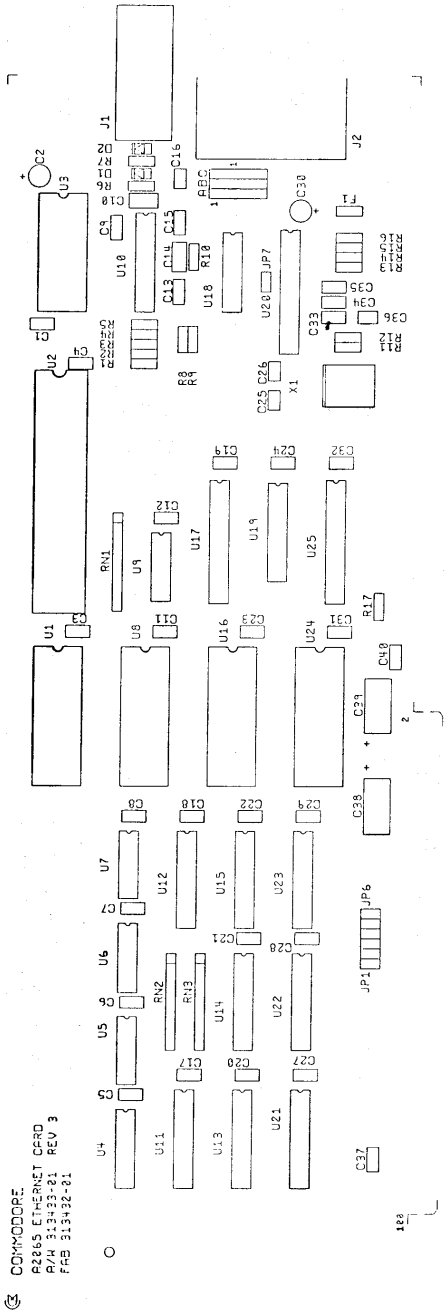
532065-01	A2065 SHIPPING ASSY
363097-06	BOX INDIVIDUAL PACKING
363035-05	BOX BULK SHIPPING
363361-01	MANUAL USERS GUIDE ENGLISH
314877-04	SERVICE CENTER LIST
318290-01	WARRANTY CARD
318928-01	ANTI STATIC BAG
313430-01	PCB ASSY

Commodore International Spare Parts List
PCB Components
PCB Assembly #313430-01

Commodore part numbers are provided for reference only and do not indicate the availability of spare parts from Commodore. Industry standard parts (Resistors, Capacitors, Connectors) should be secured locally. Part number information may vary according to country, some parts may not be available in all countries.

IC COMPONENTS		
313430-01	PCB ASSY A2065 ETHERNET LAN CARD	
390586-01	74F38	U5
390092-01	74F02	U6
390198-01	74F86	U7
901521-29	74LS373	U11,U12,U14
901521-46	74LS245	U13,U21
901521-13	74LS244	U15,U23
318041-01	74F521	U22
390081-01	74F74	U9
390631-01	LSI AMD7990 LANCE	U2
390632-01	AMD7992B SIA	U20
390633-01	AMD7996 TRANSCEIVER	U10
390636-01	20L8A INTERNAL BUS CONTROL PAL	U17
390637-01	20R6A BUS CONTROL PAL	U25
390638-01	16L8B CONFIG PAL	U19
390639-01	PROM 256X4 AUTOCONFIG A2065	U4
310024-01	8K X 8 SRAM 150 NS	U1,U8,U16,U24
390640-01	LIN DC - DC CONV +5V TO −9V	U3
390641-01	TRANSFORMER PULSE 75 UH	U18
390642-01	CRYSTAL 20MHZ HC - 49/U	X1
IC SOCKETS		
904150-05	L/P 28 PIN DIP .600	U1,U8,U16,U24
904150-02	L/P 16 PIN DIP .300	U4
251313-01	DIP 48 PIN .600	U2
390060-01	DIP 24 PIN .300	U17,U20,U25
904150-08	L/P DIP 20 PIN .300	U10,U19
RESISTOR NETWORKS		
902410-07	SIP 10K OHM 10 PIN	RN1,RN3
902410-10	SIP 1K OHM 10 PIN	RN2
RESISTORS 1% @ ¼ WATT, UNLESS OTHERWISE SPECIFIED		
251575-55	METAL 40.2 OHM	R2,R3,R13-R16
251575-58	METAL 510 OHM	R11
251575-39	METAL 3K	R12
251575-54	METAL 9.09 OHM	R5,R7
251575-62	METAL 150K OHM	R1
251575-46	METAL 174 OHM	R4
251575-57	METAL 499 OHM	R8
251575-60	METAL 24.9K OHM	R9
251575-61	METAL 75K OHM	R10
251575-35	METAL 1K OHM	R6
901550-18	CF 2.2K OHM, ¼ WATT, 5%	R17

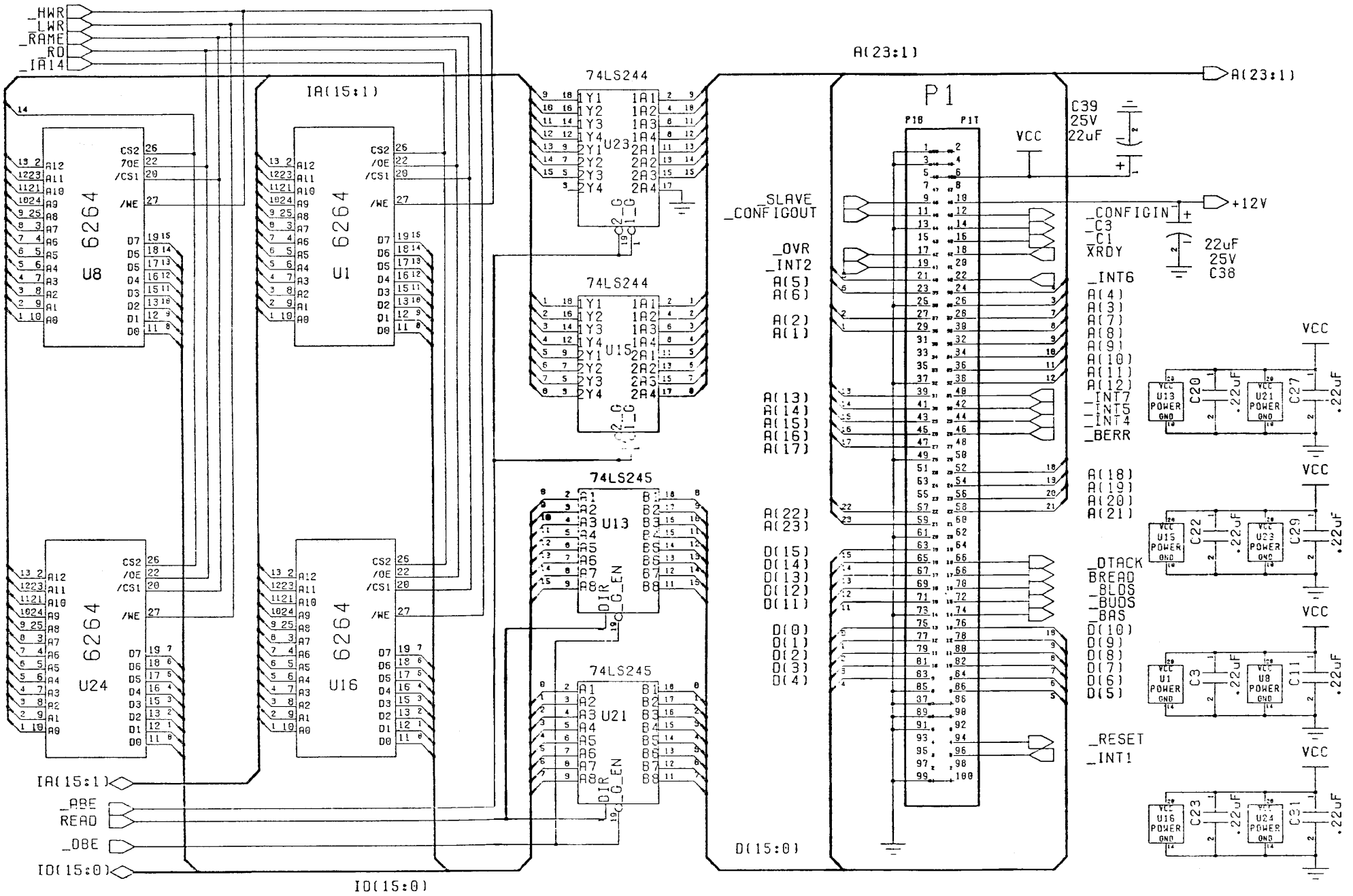
CAPACITORS		
900020-08	CER RDL .22UF 100V	C3-C8,C11,C12,C17-C24, C27-C29,C31,C32,C37, C40
900014-08	CERM RAD .1 UF MLC X7R	C1,C13,C15,C33,C35,C9
900019-15	CERM RAD 100PF MLC NPO	C25,C26
900050-28	MICA RAD 47PF NPO	C10
900019-12	CERM RAD MLC 680PF NPO	C36
900019-33	CERM RAD MLC 5600PF NPO	C34
900019-34	CERM RAD MLC 220PF NPO	C16
390646-01	CERM RAD MLC 5.0 PF NPO	C14
900101-08	ELEC AXL 22 UF 25V	C38,C39
900402-08	TANT RAD 4.7UF 25V	C30
900402-13	TANT RAD 1.0 UF 35 V	C2
CONNECTORS		
390584-02	PCB MOUNT RT/ANGLE FEMALE BNC	J1
390241-09	15 PIN DSUB RT/ANGLE FEMALE	J2
903345-06	HEADER DIL 12 PIN .100	JP1-JP6
903326-02	HEADER DIL 2 PIN .100	JP7
390043-01	SHUNT FEMALE 2 POS	JP2
390043-02	SHUNT FEMALE DIL .100 12 POS	ABC
390043-01	SHUNT FEMALE 2 POS (SUBSTITUTE FOR 390043-02)	ABC
313429-01	ETHERNET CARD BRACKET	
DIODES		
900750-02	1N4002	D1
390645-01	1N4150	D2
390280-03	FUSE .750A PICO	F1
MISCELLANEOUS		
316893-01	LABEL FCC ID A2065	
366189-01	LABEL COPYRIGHT	

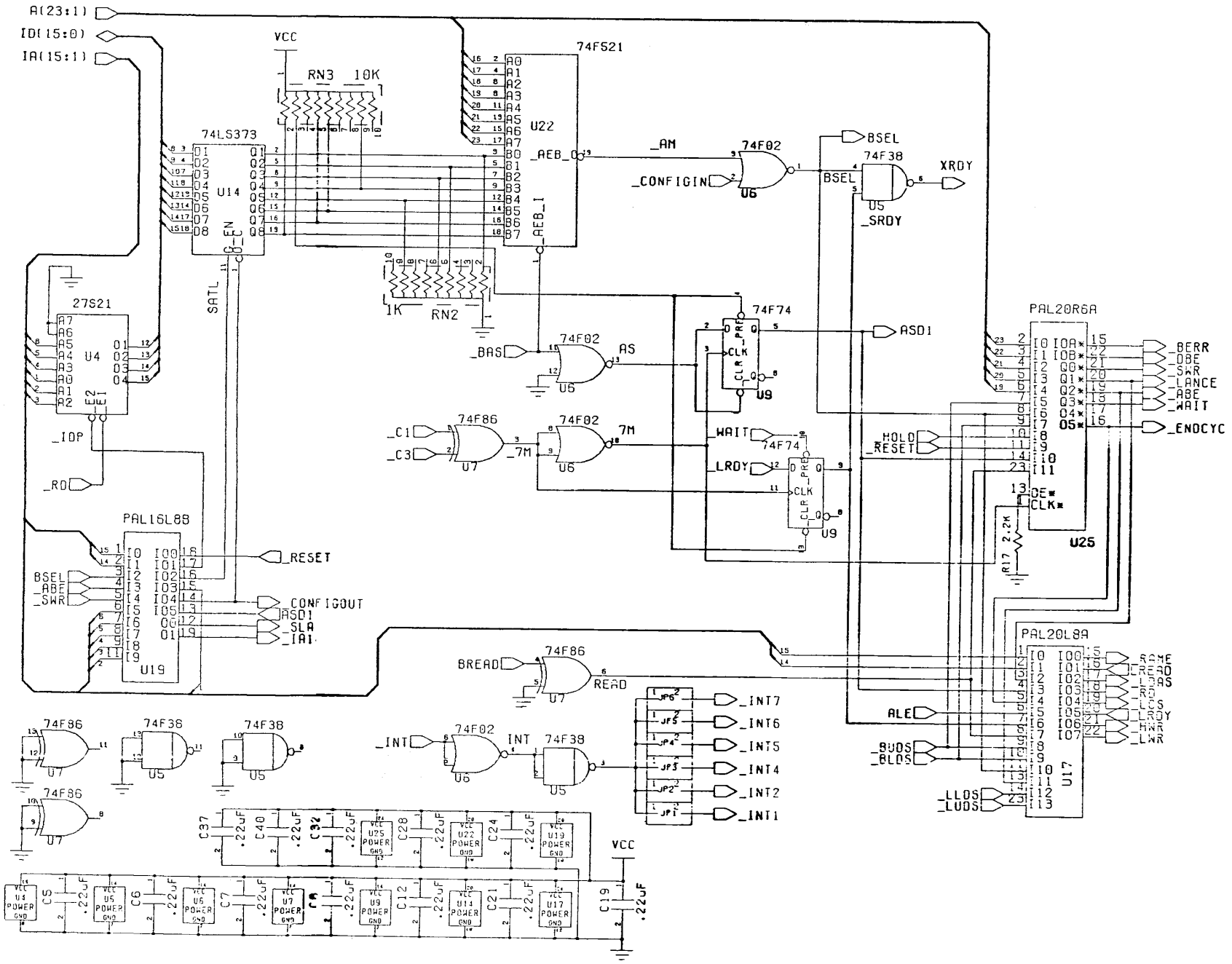


PCB BOARD LAYOUT #313433, REV. 3

Schematic #313431, Rev. A

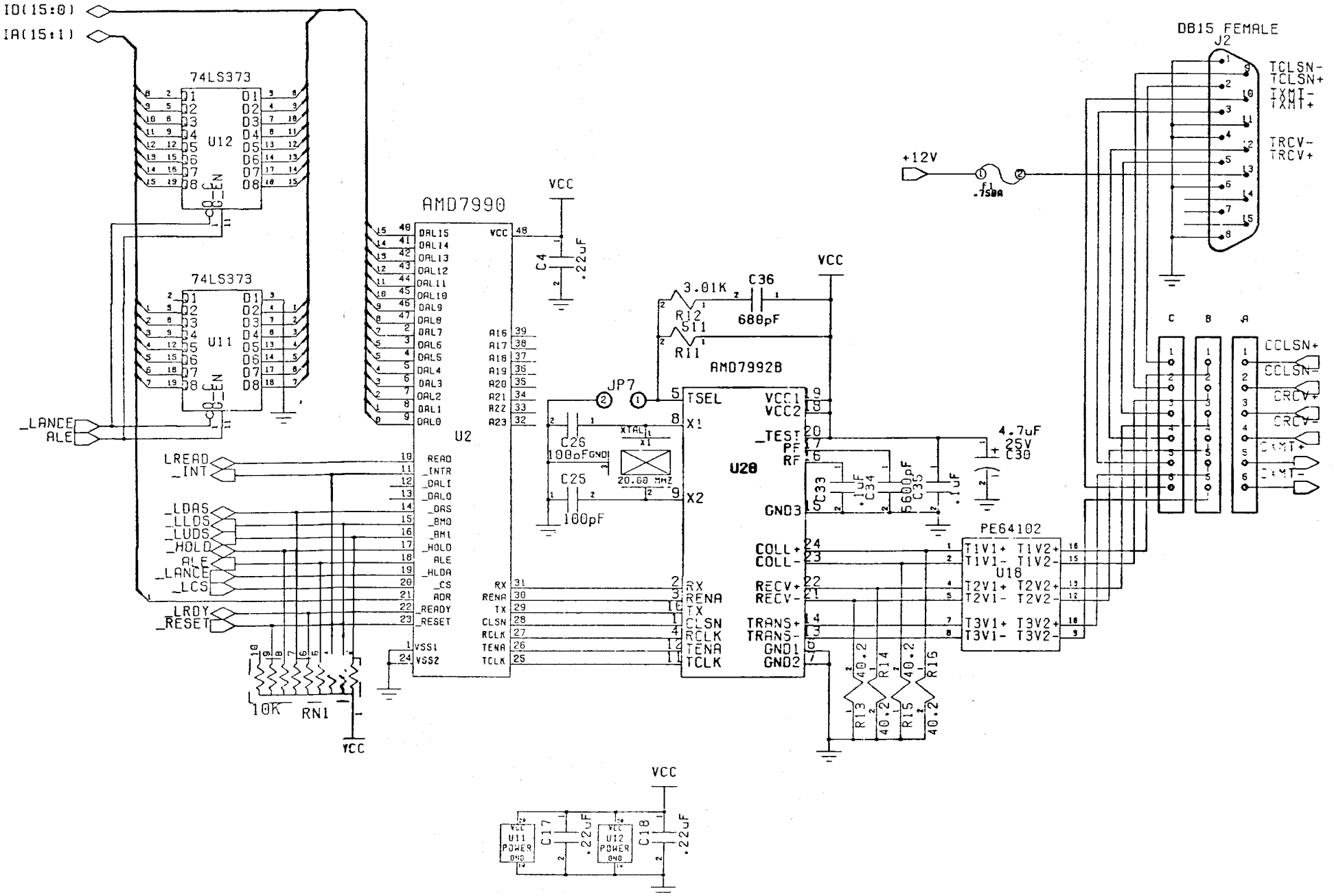
Sheet 1 of 4

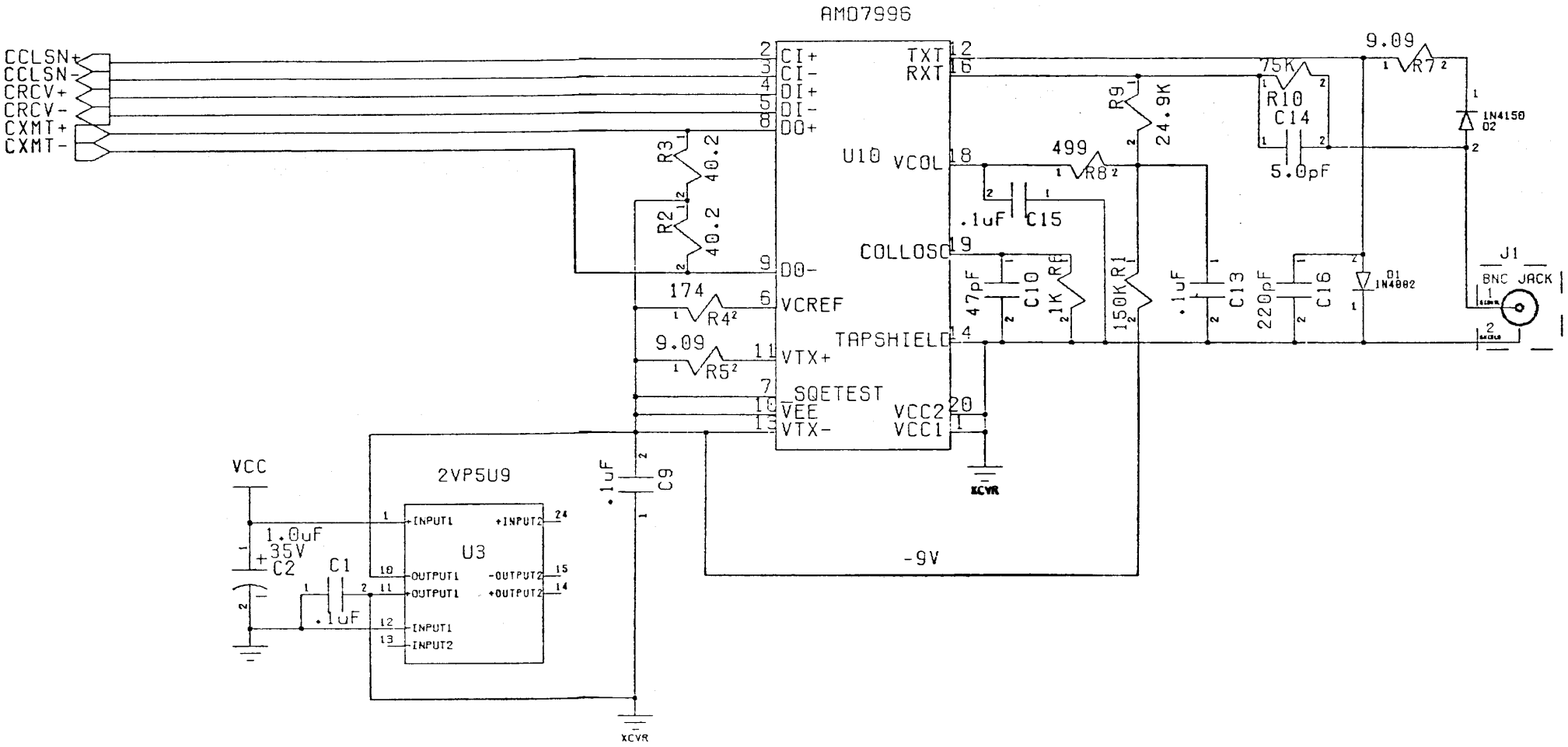



A(23:1)
ID(15:0)
IA(15:1)
VCC
RN3 10K
74LS373
U14
74F521
U22
_AEB_0
_AEB_1
_AM
74F02
_CONFIGIN
U6
BSEL
74F38
XRDY
U5
_SRDY
1K
RN2
27S21
U4
SATL
_IOP
_RD
_BAS
AS
74F74
ASD1
U9
74F86
_C1
_C3
_7M
7M
U7
WAIT
LRDY
HOLD
_RESET
PAL20R6A
U25
_BERR
_DBE
_SWR
_LANCE
_ABE
_WAIT
_ENDCYC
PAL16L8B
U19
_RESET
CONFIGOUT
ASD1
_SLA
_IA1
BSEL
_ABE
_SWR
PAL20L8A
U17
BREAD
READ
ALE
_BUDS
_BLDS
_LLDS
_LUDS
_INT
INT
_INT7
_INT6
_INT5
_INT4
_INT2
_INT1
C37 .22uF
C40 .22uF
C32 .22uF
C28 .22uF
C24 .22uF
C5 .22uF
C6 .22uF
C7 .22uF
C12 .22uF
C21 .22uF
C19 .22uF

Schematic #313431, Rev. A

Sheet 3 of 4




AMD7996
CCLSN+
CCLSN-
CRCV+
CRCV-
CXMT+
CXMT-
CI+
CI-
DI+
DI-
DO+
DO-
VCREF
VTX+
SQETEST
VEE
VTX-
TXT
RXT
VCOL
COLLOSC
TAPSHIELD
VCC2
VCC1
U10
R3 40.2
R2 40.2
174 R4
9.09 R5
499 R8
24.9K R9
75K R10
9.09 R7
C14 5.0pF
.1uF C15
47pF C10
1K R6
150K R1
.1uF C13
220pF C16
D1 IN4002
1N4150 D2
J1 BNC JACK
XCVR
VCC
2VP5U9
U3
INPUT1
+INPUT2
OUTPUT1
-OUTPUT2
+OUTPUT2
1.0uF 35V C2
C1 .1uF
.1uF C9
-9V